IN THE CLAIMS:

Please cancel, without prejudice, claims 1-7 in the underlying PCT application. Please also cancel, without prejudice, claims 1-7 in the annex to the International Preliminary Examination Report ("IPER").

Please add the following new claims:

8. (New) A method for testing a digital protective circuit, comprising:

outputting digital current and voltage signals in cycles by a data processor to simulate a current and voltage response of a power supply network;

buffering consecutively the output digital current and voltage signals;

upon reaching a specific quantity of buffered digital current and voltage signals, outputting oldest ones of the buffered digital current and voltage signals in cycles;

rebuffering newer ones of the digital current and voltage signals;

generating corresponding currents and voltages from the output oldest ones of the digital current and voltage signals;

supplying the corresponding currents and voltages to the protective circuit;

detecting tripping signals from the protective circuit;

upon an occurrence of a tripping signal, outputting by the data processor network error-specific digital current and voltage signals while the oldest ones of the digital current and voltage signals continue to be output in cycles; and

buffering the output network error-specific digital current and voltage signals.

9. (New) The method according to claim 8, further comprising:

determining the specific quantity of digital current and voltage signals buffered as a function of a response time of switches for which the protective circuit is used, taking a cycle time into account.

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10. (New) The method according to claim 8, wherein the buffered digital current and voltage signals are output at an interval that corresponds to a duration of a tripping signal-free test period needed to output further buffered digital current and voltage signals.

11. (New) The method according to claim 8, wherein the buffered digital current and voltage signals are output at an interval that is greater than a duration of a tripping signal-free test period needed to output further buffered digital current and voltage signals.

12. (New) An arrangement for testing a digital protective circuit, comprising:

a data processing system to simulate a current and voltage response of a power network using a network model by outputting digital current and voltage signals in cycles;

a buffer assigned to the data processing system in which the output digital current and voltage signals are buffered consecutively, wherein, upon reaching a specific quantity of buffered digital current and voltage signals, oldest ones of the buffered digital current and voltage signals are output in cycles, newer ones of the buffered digital current and voltage signals being rebuffered;

a converter unit located downstream from the data processing system, the converter unit to generate corresponding currents and voltages from the output oldest ones of the digital current and voltage signals and to supply the corresponding currents and voltages to the protected circuit; and

a sensing arrangement assigned to the protective circuit, the sensing arrangement triggering the data processing arrangement to output network error-specific digital current and voltage signal from the protective circuit.

13. (New) The arrangement according to claim 11, wherein the buffer is sized to buffer all digital current and voltage signals output during a tripping signal-free test period corresponding to a response time of switches provided for interaction with the protective circuit.

14. (New) The arrangement according to claim 11, wherein the buffer is a ring buffer.

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